The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NIR YONA, YOSEF BEN MOSHE, DORI ITZHAKI, MICHAEL FELDMAN, GIDI NAVON, and JACOB SHIMONI

Appeal No. 2004-1036
Application No. 09/544,054

ON BRIEF

Before, KRASS, FLEMING and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-11, 13-29, and 31-38. Claims 12 and 30 have been indicated by the examiner as being directed to allowable subject matter and form no part of this appeal.

The invention pertains to local area network (LAN) modular switches. In particular, a modular switch includes a plurality

of cards to which computers or other devices connect. The switch also includes a plurality of sub-buses which are used for communication between cards. A controller keeps track of current bandwidth needs of the cards and allocates the sub-buses to the various cards based on this need.

Representative independent claims 1 and 13 are reproduced as follows:

1. A modular switch, comprising:

a plurality of backplane sub-buses;

a plurality of cards which are each allocated one or more of the backplane sub-buses; and

a controller which dynamically allocates the backplane sub-buses to the plurality of cards, based on bandwidth needs of the cards.

13. A modular switch, comprising:

a plurality of backplane sub-buses; and

a plurality of cards which are configurable to listen to a variable number of the backplane sub-buses.

The examiner relies on the following references:

Prince et al.	5,734,656	Mar. 31, 1998
Ha-Duong	5,768,270	Jun. 16, 1998
LaBerge	5,771,358	Jun. 23, 1998
Riley	5,875,351	Feb. 23, 1999
Fan et al. (Fan)	6,219,706	Apr. 17, 2001 (filed Oct. 16, 1998)
Porter et al. (Porter)	WO 93/15464	Aug. 5, 1993

In addition, the examiner relies on appellants' admitted prior art (APA) at page 2, lines 6-9, of the instant specification, viz., ". . . in some cases it is desired to form separate connections using different protocols, such as Ethernet and ATM, which cannot be interconnected without signal conversions. A simple solution is to create separate networks using a plurality of different switches which are not interconnected. . . ."

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as anticipated by Prince. Claims 13, 14, and 16-18 stand rejected under 35 U.S.C. § 102(b) as anticipated by Porter. Claims 23-29 stand rejected under 35 U.S.C. § 102(b) as anticipated by LaBerge.

In addition, claims 4-11, 15, 19-22, and 31-38 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites Porter with regard to claim 19, adding LaBerge with regard to claim 15, Fan with regard to claims 20 and 21, Ha-Duong with regard to claim 22, LaBerge with regard to claims 31-33 and 35-37, and adding APA to this last combination with regard to claim 34. With regard to claim 38, the examiner cites Porter, LaBerge and Riley.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

REJECTIONS UNDER 35 U.S.C. § 102(b)

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

Regarding claims 1-3, the examiner asserts that Prince discloses a modular switch, at element 200 in Figure 2, and that this "switch" comprises a plurality of backplane sub-buses, identified as cell slots in Figure 7, i.e., time dimension multiplexing buses of an ATM switching backplane bus. The examiner cites column 7, lines 33-37, of Prince. The examiner further cites LAN modules 201-204 and ATM module 206 of Prince's Figure 2, as the claimed "plurality of cards which are each allocated one or more of the backplane sub-buses" (referring to column 12, lines 36-40) and the examiner cites master controller processor (MCP) 430, of Figure 4, as the claimed "controller which dynamically allocates the backplane sub-buses to the

plurality of cards, based on bandwidth needs of the cards" (referring to column 12, lines 32-35, and column 13, lines 41-46, of Prince.

Appellants argue that Prince does not disclose the claimed plurality of sub-buses because this limitation is not met by slots of a time domain multiplexed bus, as alleged by the examiner. This is so, asserts appellants, because the instant specification makes clear, at page 1, lines 26-32, that the term "sub-bus" as used in the instant claims refers to something other than a slot or set of slots of a time domain multiplexed bus.

We have reviewed the cited portions of the specification. While it is clear, from the specification that appellants' invention seeks to overcome the "slow and complex" nature of using time domain multiplexing which divides a bus into slots and allocates an amount of slots to a transmitter for transmitting data, we find nothing in the language of claims 1-3 that distinguishes "a plurality of backplane sub-buses" over the cell slots of Prince, or even over the use of the term "sub-buses" recognized by appellants, themselves, wherein "sub-buses are allocated to. . . cards using time domain multiplexing" (specification-page 1, line 27).

The cell slots of Prince are just those types of "sub-buses" referred to by appellants in the background section of their

specification, at page 1, and, even though we realize that appellants seek to improve this prior art, we find no distinguishing language in claims 1-3 and we find no reason not to give the term "plurality of backplane sub-bases" its ordinary and recognized meaning in the art as permitting this to describe elements allocated to cards using time domain multiplexing, as provided at page 1 of the instant specification.

While appellants rightly contend that they can be their own lexicographer, we find no specific definition of the term "sub-buses," within the specification, which comports with appellants' view that the cell slots in Prince cannot meet appellants' definition of "sub-buses."

Appellants argue, e.g., page 4 of the reply brief, that their claimed sub-buses are "physical portions of a given bus," and not time slots. Again, we find no language in claims 1-3 which sets forth that the plurality of backplane sub-buses are physical portions of a given bus, nor do we find any language in those claims precluding time slots from constituting the plurality of sub-buses.

Accordingly, we will sustain the rejection of claims 1-3 under 35 U.S.C. § 102(b) as anticipated by Prince.

Turning to the rejection of claims 13, 14 and 16-18 under 35 U.S.C. § 102(b) over Porter, the examiner contends, with

regard to independent claim 13, that Porter discloses a modular switch (backplane 20 with line switches in Figure 2) comprising a plurality of backplane sub-bases (pointing to N switched lines of Figure 3 and citing page 7, lines 19-23 and page 14, lines 20-23) and a plurality of cards (identified as "boards," and referring to page 1, lines 9-10, and page 3, lines 21+) which are configurable to listen to a variable number of said backplane sub-buses (pointing to page 4, lines 2-9, and page 15, line 25 through page 16, line 2).

Similar to the argument supra, appellants contend that Porter is directed to a single physical bus and therefore cannot anticipate a "plurality of backplane sub-buses." Specifically, appellants argue, at page 5 of the reply brief, that the N switched lines in Figure 3 of Porter "comprise the entire backplane bus which is N lines wide" (reply brief-page 5). Moreover, contend appellants, if the plurality of cards corresponds to Porter's boards, as argued by the examiner, such boards are not disclosed as being reconfigurable in the manner claimed since Porter teaches to utilize a separate switch array between the backplane bus and the boards, referring to page 7, lines 1-5, of Porter. Thus, appellants argue that the switch array in Porter is not part of any of the boards and, therefore,

the boards in Porter are not configurable in the manner claimed (reply brief-page 6).

For the reasons supra, we find that the N switched lines of Porter may, indeed, be considered to be "sub-buses," as claimed. As to appellants' argument that the "boards" in Porter are not "configurable to listen to a variable number of the backplane sub-buses," we disagree. As stated in Porter, and cited by appellants at page 6 of the reply brief, the plurality of slots connect to the lines and provide connections with the plurality of boards. Further, there is a condition-variable switch array between the lines and each slot. While the switch array, per se, of Porter may not be part of the boards, the connectability of the slots is controlled and, since the boards are connected to the slots, the connectability of the boards may also said to be controlled, or reconfigured, so that each board's communication with other boards is controlled. Therefore, it seems fair to say that Porter's boards are configurable to listen to a variable number of the backplane sub-buses, as claimed.

Accordingly, we will sustain the rejection of claims 13, 14, and 16-18 under 35 U.S.C. § 102(b) as anticipated by Porter.

Turning to the rejection of claims 23-29 under 35 U.S.C. § 102(b) as anticipated by LaBerge, the examiner contends, with regard to independent claim 23, that LaBerge discloses a method

for allocating sub-buses, i.e., apportioning bus bandwidth (column 1, lines 6-8) to cards (bus requesters 26, 28, 30, 32 of Figure 1) of a switch (bus controller 24 in Figure 1) comprising determining bandwidth needs of each of the cards (Figure 3 and column 5, lines 9-26), assigning each of the cards a bus demand value (weighting value) which is a function of (column 3, lines 35-36) the bandwidth needs of the card and a current bandwidth allocated to the card (Figures 2-3 and column 3, lines 45+), and allocating (apportioning) the sub-buses (bus bandwidth) to the cards (bus requesters) based on the bus demand values of the cards (column 3, lines 36-44, and column 4, lines 21-28).

Again, appellants argue that LaBerge fails to disclose a plurality of sub-buses. Moreover, appellants argue, at page 6 of the reply brief, that if the bus controller 24 of LaBerge corresponds to the switch of claim 23, then the bus requesters 26, 28, 30, and 32 are not "cards of a switch," as required by the claims. Appellants point out that these bus requesters are all external to the bus controller 24, and represent main memory, hard drive A, hard drive B, and PCI elements, respectively, of a computer system, referring to column 2, lines 33-34, and 46-47 of LaBerge. It is appellants' contention that these standard computer elements cannot reasonably be construed as being anticipatory of "cards of a switch," as claimed.

As discussed supra, we find that different time/space allocations on a system bus may be considered to be "sub-buses" of that bus. Therefore, we do not find persuasive appellants' argument that LaBerge fails to disclose a plurality of sub-buses.

We do find persuasive, however, appellants' argument that the standard computer elements 26, 28, 30, and 32, said to be "cards," as claimed, by the examiner, cannot reasonably be construed as being anticipatory of "cards of a switch," as claimed. This argument appears to have been raised for the first time in the reply brief, and we have no response from the examiner as to why these elements should be considered "cards." One might argue that it was well known that memory and video controllers, for example, may be provided on circuit "cards," but it does not appear to us that hard drive A and B, elements 28 and 30, respectively, in LaBerge, would normally be considered "cards," let alone "cards of a switch," as claimed. Since the examiner has identified controller 24 as the claimed "switch" and elements 26, 28, 30 and 32 as comprising the claimed "cards," in accordance with the language of claim 23, elements 26, 28, 30 and 32 must be "cards of a switch," i.e., part of controller 24. This is clearly not the case, as far as we can discern from LaBerge's disclosure, since elements 26, 28, 30 and 32 appear to be separate from controller 24 and the examiner has not shown any

disclosure in LaBerge suggesting that elements 26, 28, 30 and 32, together with controller 24, may all be on one chip, or "card."

Because the examiner has not explained why the computer elements of LaBerge should be considered to be "cards," as claimed, and LaBerge does not describe these elements as "cards," it would be speculative, at best, to find that the elements identified in LaBerge by the examiner as "cards" meet the terms of claim 23. While "cards" is a very broad term, the examiner was still required to give it some meaning and to show that the elements of the reference comported with that meaning, yet the examiner has not done so.

It might very well be that a case for obviousness could be made since LaBerge teaches a method of allocating sub-buses, or portions of a system bus, to elements of a computer system and, perhaps, some analogy may be made between these computer elements and "cards of a switch," but the instant rejection is under 35 U.S.C. § 102(b), based on anticipation, and not under 35 U.S.C. § 103 for obviousness, nor has the examiner made an alternative rejection of claims 23-29 under 35 U.S.C. § 103.

Accordingly, we will not sustain the rejection of claims 23-29 under 35 U.S.C. § 102(b) as anticipated by LaBerge.

REJECTIONS UNDER 35 U.S.C. § 103

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teachings, suggestions or implications in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts

to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1040, 228 USPQ 685, 687 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 146-147 (CCPA 1976). Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered and are deemed to be waived [see 37 CFR 1.192 (a)].

It appears to us, from a review of the examiner's answer, that the examiner has explained each and every rejection under 35 U.S.C. § 103, including a rationale for the combinations of references and as to why the artisan would have found the claimed subject matter obvious thereover, i.e., the examiner has set forth a prima facie case of obviousness.

Yet, appellants' response to the rejections under 35 U.S.C. § 103, in paragraphs titled Issue 4 through Issue 16, at pages 7 through 11 of the principal brief, is merely to rely on the arguments made against the rejections under 35 U.S.C. § 102(b) (viz., that the primary references lack a teaching of a plurality of sub-buses), or to make general statements as to how the

examiner has failed to show objective evidence of motivation to combine the references.

Appellants' arguments are not persuasive because, as discussed supra, we do not agree with appellants regarding the teaching of a plurality of sub-buses in the primary reference. Moreover, general arguments as to a lack of motivation to combine, without a corresponding specific allegation as to particular errors in the examiner's rationale, are not persuasive, especially where, as here, the examiner has provided some reason for making the combinations and appellants have shown no error in such reasoning.

In the reply brief, appellants get a bit more specific. At page 7 therein, appellants argue that the examiner's rejection of independent claim 31 under 35 U.S.C. § 103 over Porter in view of LaBerge is in error because Porter is directed to a computer backplane having line switches while LaBerge is directed to a processor bus shared by a plurality of processors in a computer system. Thus, appellants conclude, "[c]ollectively, the references simply fail to disclose an arrangement in which backplane sub-buses of a modular switch are allocated to communication cards of the modular switch based on bus demand values of the cards" (reply brief-page 7).

We agree with the examiner. It is true that LaBerge does not teach a plurality of communication cards, but rather a plurality of computer elements (memory, hard drives, video controller) which are granted certain bandwidth portions. However, Porter is cited by the examiner for the teaching of the subject matter of claim 31 but for the controller being further configurable to allocate the sub-buses to the cards based on bus demand values of the cards. Even though LaBerge does not show the claimed cards, it does teach that sub-buses, or bus allocation, are granted to certain elements based on bus demand values of those elements. This is taught, for example, at column 3, lines 33-36, of LaBerge, regarding the calculation of a weighting value for each bus requester. Since both Porter and LaBerge are concerned with apportioning bandwidth of a system bus, the artisan would have found it obvious to employ the advantageous apportionment method of LaBerge in the bandwidth apportionment method of Porter.

Appellants' arguments, at pages 7-8 of the reply brief, would appear to be emphasizing the noncombinability of the references because the bus requesters of LaBerge are elements of a computer system which would presumably already be present in Porter's processing unit(s) 11. However, the combinability of the references, within the meaning of 35 U.S.C. § 103, is not

based on the bodily incorporation of one reference into the other. It is based, rather, on what the totality of the teachings of the references would have suggested to the skilled artisan in the art of bus allocation. We find that while Porter teaches the bulk of the claimed subject matter, LaBerge's teaching of allocating a bus to a plurality of elements based on bus demand values of those elements would have led the artisan to modify Porter to include LaBerge's method of allocation whereby Porter's controller may be further configurable to allocate the sub-buses, or lines, to Porter's boards (cards) based on bus demand values of the boards.

Therefore, we will sustain the rejection of claims 31-33 and 35-37 under 35 U.S.C. § 103.

Since claims 34 and 38 depend from independent claim 31 and appellants do not specifically argue the merits of these claims separate from claim 31, we will also sustain the rejection of claims 34 and 38 under 35 U.S.C. § 103.

We will also sustain the rejection of claims 4-11 under 35 U.S.C. § 103 since appellants do not argue the merits of these claims separately from independent claim 1.

Moreover, we will also sustain the rejection of claims 15 and 19-22 under 35 U.S.C. § 103 since appellants do not argue the

merits of these claims separate from independent claim 13 and dependent claims 14 and 16-18.

CONCLUSION

We have sustained the rejection of claims 1-3, 13, 14, and 16-18 under 35 U.S.C. § 102(b) but we have not sustained the rejection of claims 23-29 under 35 U.S.C. § 102(b).

We have also sustained the rejection of claims 4-11, 15, 19-22, and 31-38 under 35 U.S.C. § 103.

Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS)
Administrative Patent Judge)
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MICHAEL R. FLEMING)BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
)INTERFERENCES
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)
)
JOSEPH L. DIXON)
Administrative Patent Judge)

EK/RWK

JOSEPH B. RYAN
RYAN, MASON & LEWIS, LLP
90 FOREST AVENUE
LOCUST VALLEY, NY 11560